

Path to PDR

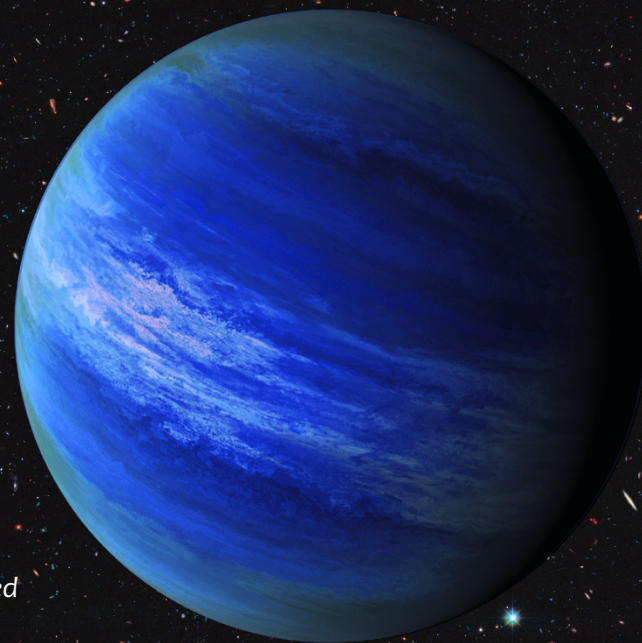
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CGI Manager

24 Oct 2018

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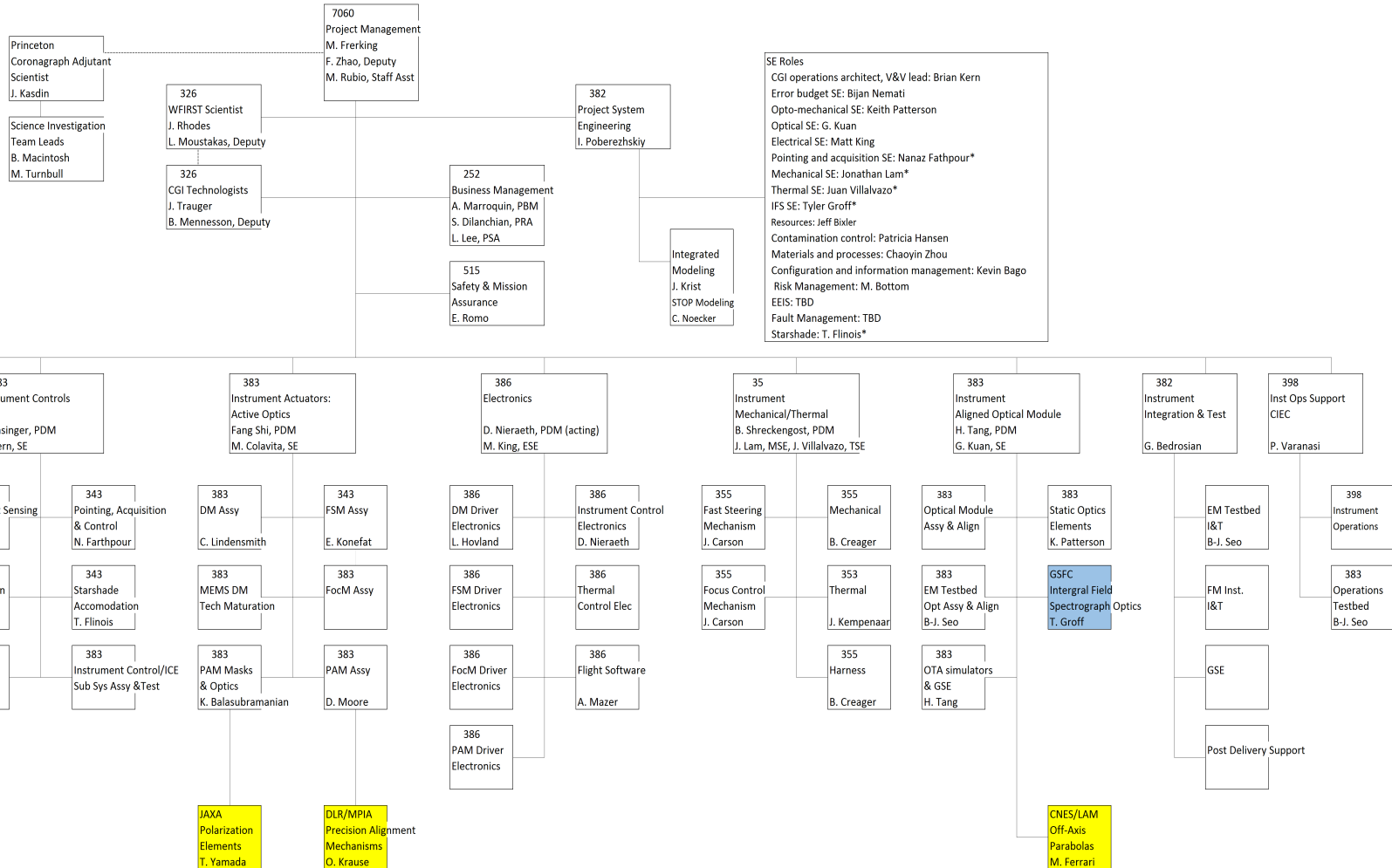


- Refine operations concept
- Develop calibration approach and requirements
- Refine requirements and flowdown
- Define interfaces
- Bound risk on technology development
- Develop preliminary design
 - Make key decisions following trades
 - Document designs in preparation of fabricating Engineering Models (EMs)
 - Definitize international contributions
 - Conduct Integrated Modeling in collaboration with WFIRST project
- Support project and instrument PDRs
- Baseline technical implementation and programmatic commitments

WFIRST

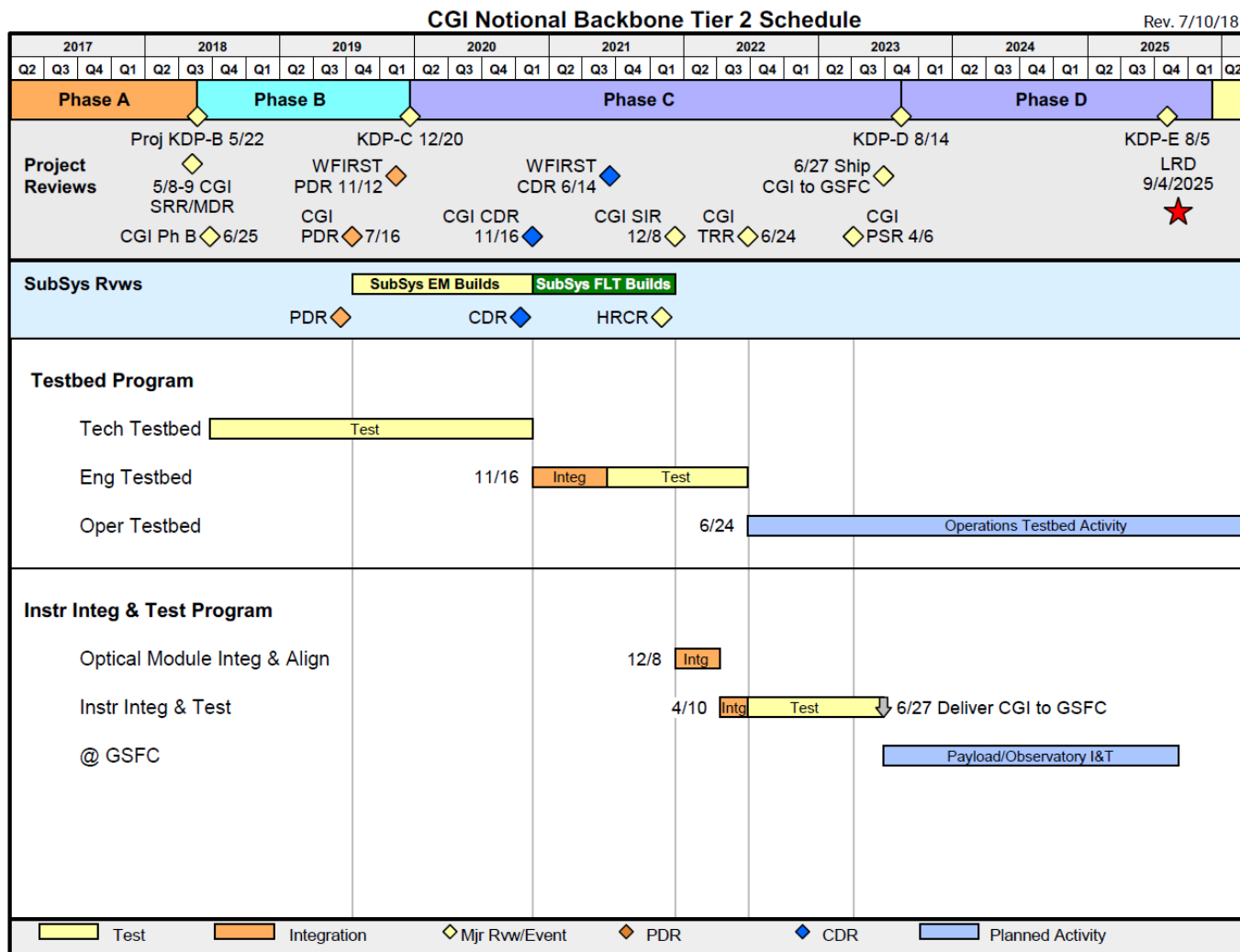
WIDE-FIELD INFRARED SURVEY TELESCOPE
ASTROPHYSICS • DARK ENERGY • EXOPLANETS

Phase B/C/D Organization Chart

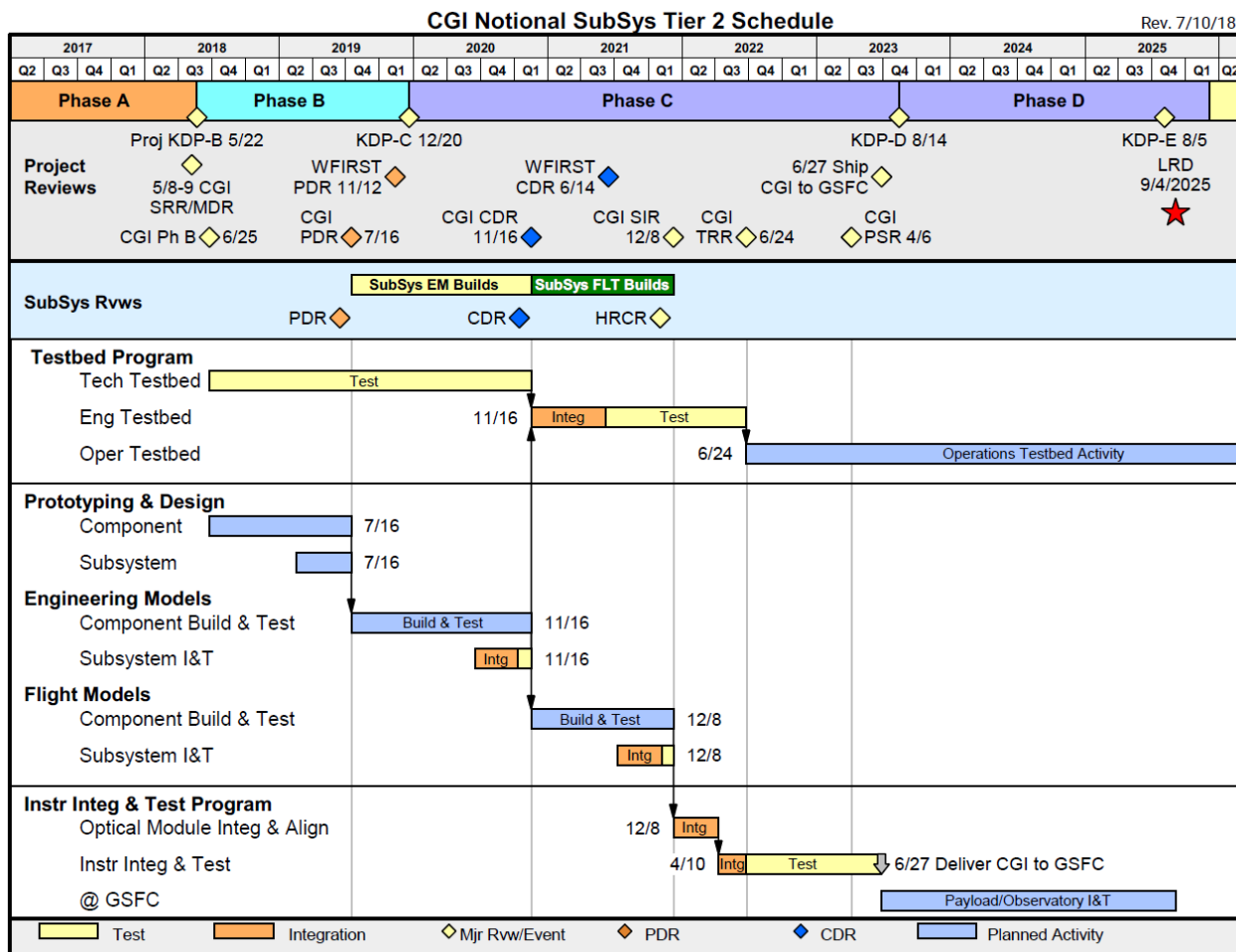


System Level Activities

- Life cycle schedule is architected around system level activities
- Subsystem EM build occurs between PDR and CDR
- Subsystem Flight build occurs between CDR and SIR



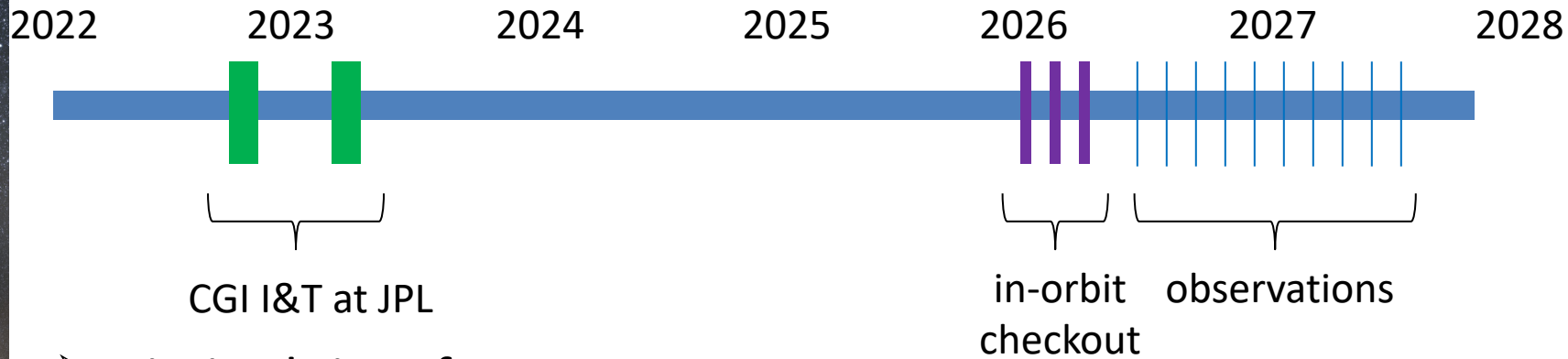
Subsystem Activities



- Subsystem design and prototyping occurs prior to PDR
- Subsystem EM build occurs between PDR and CDR
- Subsystem Flight build occurs between CDR and SIR

- Finalize approach for managing TCA Pupil/CGI interface
- Prove out on-board HOWFS and LOWFS algorithms with prototypes
- Downselect to Deformable Mirror design
- Downselect to EMCCD design
- Design for PAMs – well defined plan with MPIA/DLR

CGI Wavefront Control (WFC)



➤ Limited time for WFC

- 2 weeks per mode (3 modes) on the ground
- Entire CGI in-orbit checkout in 19 days
 - First time WFC L3 requirement: 150 hrs per mode
- Repeat L3 WFC requirement at the beginning of each CGI observation: 30 hr for each mode

➤ On-board Jacobian calculation: 2d requirement, 0.5d CBE

➤ A major focus of CGI activities to PDR and beyond is to confirm that we can perform wavefront control on orbit in the allocated time

Timing budget

Timing of operations is responsive to two L3 requirements:

Req.	Name	Primary Text
CGIS -511	CGI Initial On-Orbit Calibration	CGI shall be able to perform initial on-orbit calibration of each coronagraphic mode in <150 hours, pointing at a V = 2 mag star.
CGIS -512	CGI Regain Calibration	CGI shall be able to regain calibration of each coronagraphic mode previously calibrated on orbit in <30 hours, pointing at a V = 2 mag star.

To show we meet these, we have a timing budget that incorporates times for exposure (based on CGI flux calculations), calculation (based on hardware benchmarks), hardware motion and response (based on requirements), and number of iterations.

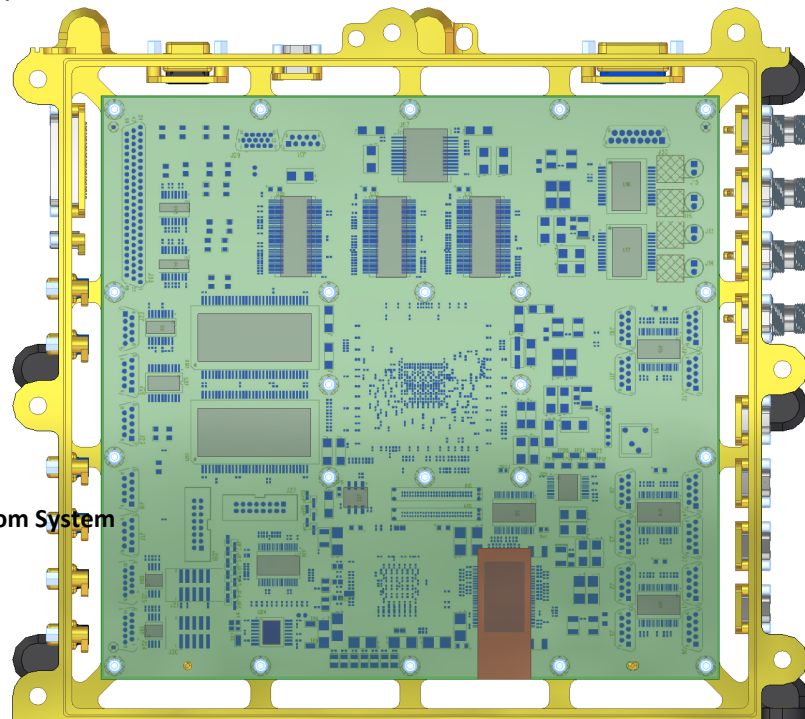
Narrow FoV	
Commissioning	
Requirement	150.0 hours
Current Best Estimate	61.0 hours
Reserve	89.0 hours
Turn-on allocation	1.6 hours
Health checkout allocation	7.4 hours
Alignment and calibration	11.3 hours
Jacobian computation	24.0 hours
Initial nulling	16.8 hours
Revisit	
Requirement	30.0 hours
Current Best Estimate	6.6 hours
Reserve	23.4 hours
Realignment	2.8 hours
Revisit nulling	3.8 hours

Wide FoV	
Commissioning	
Requirement	150.0 hours
Current Best Estimate	75.8 hours
Reserve	74.2 hours
Turn-on allocation	1.6 hours
Health checkout allocation	7.4 hours
Alignment and calibration	12.1 hours
Jacobian computation	47.3 hours
Initial nulling	7.5 hours
Revisit	
Requirement	30.0 hours
Current Best Estimate	8.1 hours
Reserve	21.9 hours
Realignment	5.3 hours
Revisit nulling	2.9 hours

Spectroscopy	
Commissioning	
Requirement	150.0 hours
Current Best Estimate	100.1 hours
Reserve	49.9 hours
Turn-on allocation	1.6 hours
Health checkout allocation	7.4 hours
Alignment and calibration	12.2 hours
Jacobian computation	26.2 hours
Initial nulling	52.8 hours
Revisit	
Requirement	30.0 hours
Current Best Estimate	20.7 hours
Reserve	9.3 hours
Realignment	5.3 hours
Revisit nulling	15.5 hours

➤ Plan to use WFIRST processor board (same as used by WFI and S/C) with LEON 4 processor and RTG4 FPGA

- Cobham GR740 Quad Core Leon 4 Processor ASIC
 - 256 MiB, 100MHz, SDRAM Code Space, (+125 Mbytes use for ECC)
 - 250 MHz internal system clock
 - 2 MiB L2 Cache (first flight processor with L2 Cache)
 - 64 KiB SUROM
 - 8 Port SpaceWire router
 - 1 MIL-STD-1553B bus
 - 2 CAN 2.0 Buses, 1 I2C Master, 2 UART over RS-422
 - 32 Bit, 33MHz PCI Host
 - SpaceWire, and JTAG Debug Interfaces
- Microsemi RTG4 FPGA
 - 4 Independent SpaceWire Ports
 - Mission Elapsed Timer (MET), and 1.X Hz Time Distribution to/from System
 - 32 Bit, 33MHz PCI Target
 - 6 GB DDR2 Memory (2 GB used for ECC)
 - 1 MIL-STD-1553B bus
 - 2 16-MiB banks of MRAM for Program Code Storage
 - UART over RS-422 and JTAG Debug Interfaces



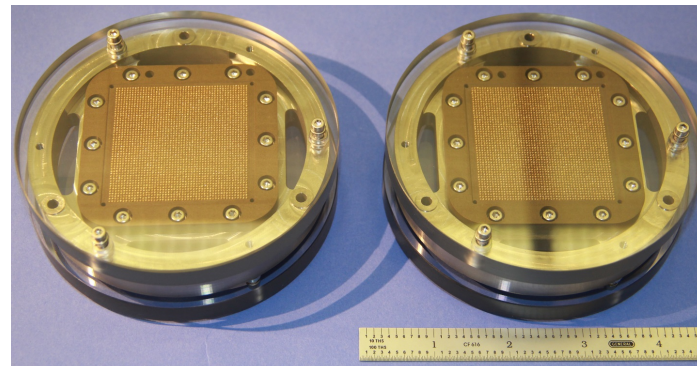
Work through PDR

- Benchmark on prototypes of baselined flight hardware (Leon 4 and FPGA) running key parts of HOWFC algorithm (EFC)
 - Focus on FFTs for Jacobian re-computations and matrix inversions done every EFC iteration
- CGI algorithms and ground calibrations for each mode allow converging
 - in the required number of iterations
 - with the required number of Jacobian recomputations

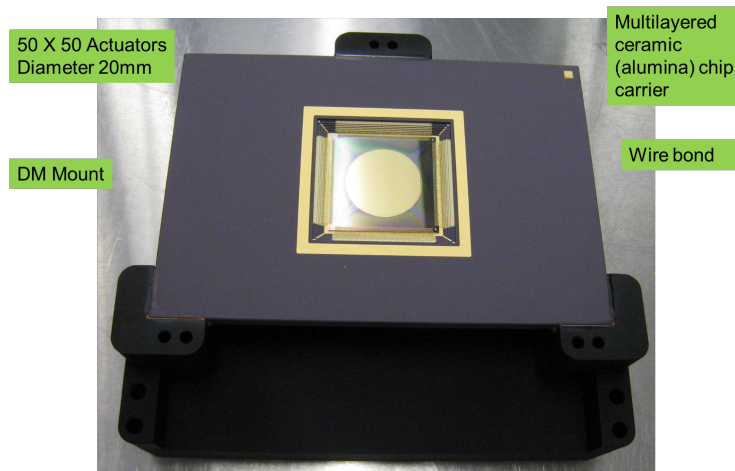
DM Trade

- CGI DM trade between AOX and BMC DMs initially performed and documented by Duncan Liu in 2014
- AOX DMs were selected at the time based on being the only ones meeting all musts:
 - All actuators operational in 48x48 circle
 - Schedule
- Since 2014:
 - BMC has made a lot of progress with their MEMS DMs
 - AOX DM flight connectorization / TRL6 demo schedule stretched out
 - Much better understanding of each DM's performance and effect on operations, assessed in context of CGI error budget and con-ops
- An updated trade was deemed appropriate...

Fuzz Button Array for AOX DM



BMC DM with wire bonds



Musts:

- Can meet schedule to TRL6 demo and flight units (Fang to cover in following slides)
- Can meet
 - DM performance requirements (in Doors NG for AOX, Brian making minor updates for BMC to be completed by the end of October)
 - Mission assurance requirements

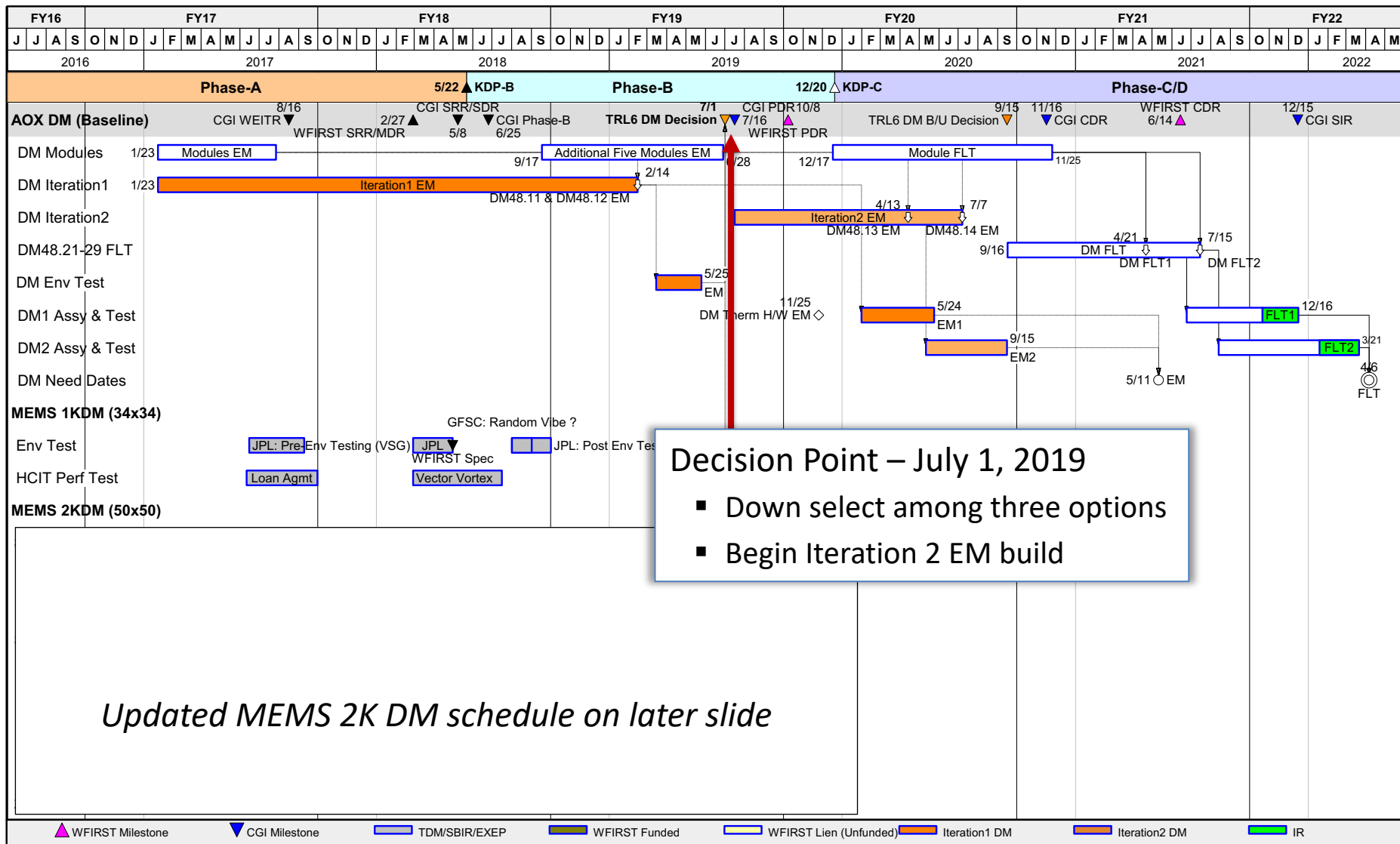
Wants (not a complete list):

- **DM thermal stability:** largest element of CGI performance budget, tightest thermal stability requirement on CGI
 - BMC+
 - **DM non-thermal settling time:** limits con-ops, speed of recovery from single event upsets in driver electronics
 - BMC+
 - **Operational robustness:** is there voltage neighbor rule to follow?
 - BMC+
 - **Larger stroke** (beyond requirement): can compensate larger OTA+TCA wavefront errors
 - BMC+
 - **Consistency of gain curve between actuators:** needs less calibration
 - BMC+
 - **Facesheet shape consistency between air and vacuum:** easier I&T
 - BMC+
 - **Handling robustness:** vulnerability to damage
 - AOX+
 - **Face sheet spatial features**
 - AOX+ (in work)
- DM element and SE will work together to put weights on each parameter in the trade and score the two DM options before PDR

TRL 6 Verification

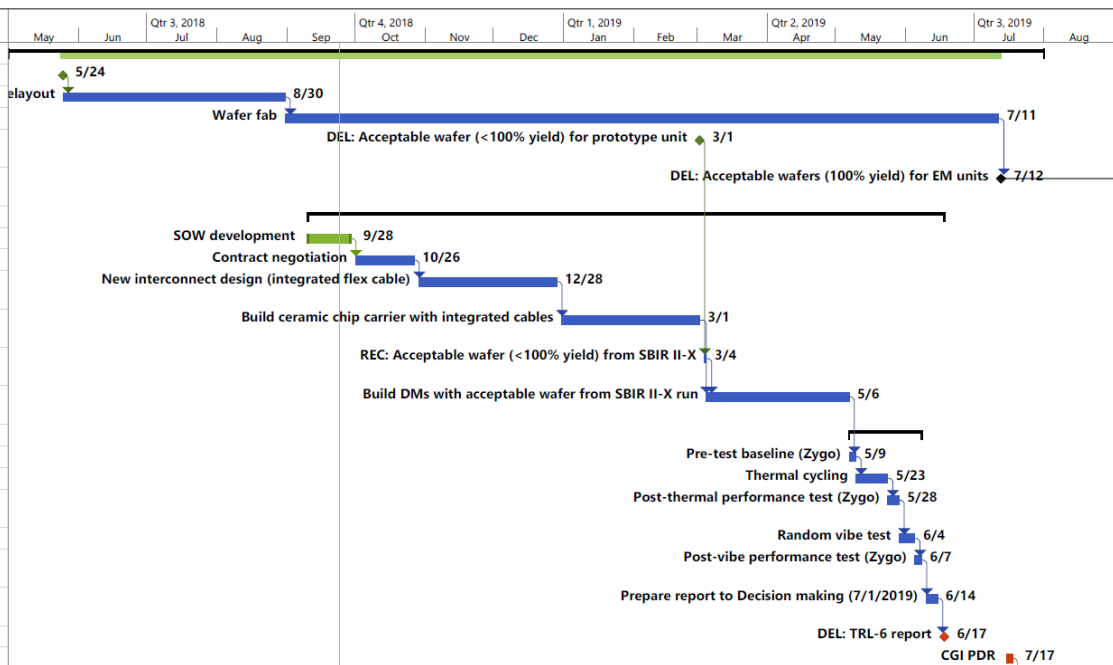
- Vibe testing of EM units to Protoflight (PF) levels
 - DM performance test before and after
 - Current DM contract has 10.8 Grms (analogy from similar programs). Awaiting traceable vibe levels.
 - Modal testing limited to sine sweep as part of random vibe
- Thermal cycling & soak of EM units to PF requirements
 - DM performance test before and after
- Performance testing includes measurement of actuator gain and stability across all actuators in the DM with DM controlled at extremes of the allowable performance range.

Primary test goal of EMs is to verify that the new interconnect design meets environmental requirements with no negative effect on DM performance



BMC MEMS DM Plan

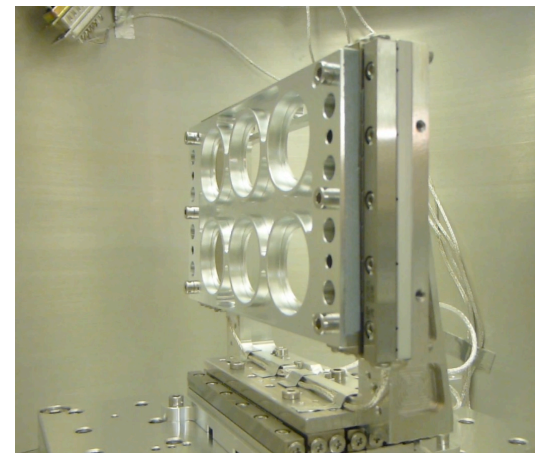
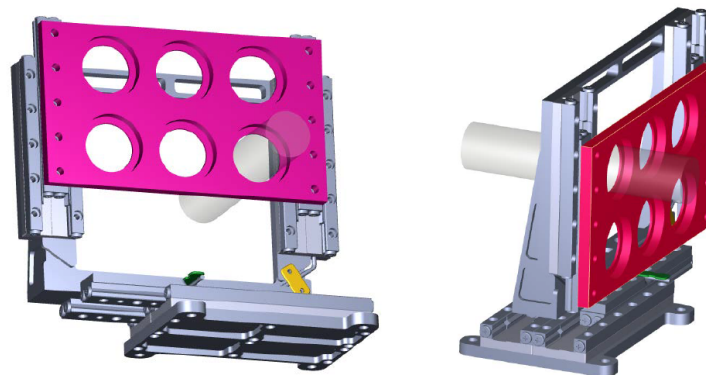
ID	Task Mode	Task Name	Duration	Start	Finish	Predecessors
1		SBIR II-X Wafer Development	327 days	Tue 5/1/18	Wed 7/31/19	
2		Kick-off	1 day	Thu 5/24/18	Thu 5/24/18	
3		Relayout	70 days	Fri 5/25/18	Thu 8/30/18	2
4		Wafer fab	225 days	Fri 8/31/18	Thu 7/11/19	3
5		DEL: Acceptable wafer (<100% yield) for prototype unit	1 day	Fri 3/1/19	Fri 3/1/19	
6		DEL: Acceptable wafers (100% yield) for EM units	1 day	Fri 7/12/19	Fri 7/12/19	4
7		Tech Maturation/Prototype	201 days?	Mon 9/10/18	Mon 6/17/19	
8		SOW development	15 days	Mon 9/10/18	Fri 9/28/18	
9		Contract negotiation	20 days	Mon 10/1/18	Fri 10/26/18	8
10		New interconnect design (integrated flex cable)	45 days	Mon 10/29/18	Fri 12/28/18	9
11		Build ceramic chip carrier with integrated cables	45 days	Mon 12/31/18	Fri 3/1/19	10
12		REC: Acceptable wafer (<100% yield) from SBIR II-X	1 day?	Mon 3/4/19	Mon 3/4/19	5
13		Build DMs with acceptable wafer from SBIR II-X run	45 days	Tue 3/5/19	Mon 5/6/19	11,12
14		Environmental tests	24 days	Tue 5/7/19	Fri 6/7/19	
15		Pre-test baseline (Zygo)	3 days	Tue 5/7/19	Thu 5/9/19	13
16		Thermal cycling	10 days	Fri 5/10/19	Thu 5/23/19	15
17		Post-thermal performance test (Zygo)	3 days	Fri 5/24/19	Tue 5/28/19	16
18		Random vibe test	5 days	Wed 5/29/19	Tue 6/4/19	17
19		Post-vibe performance test (Zygo)	3 days	Wed 6/5/19	Fri 6/7/19	18
20		Prepare report to Decision making (7/1/2019)	5 days	Mon 6/10/19	Fri 6/14/19	19
21		DEL: TRL-6 report	1 day?	Mon 6/17/19	Mon 6/17/19	20
22		CGI PDR	2 days	Tue 7/16/19	Wed 7/17/19	



- SBIR II-X: thicker wafer DM development
 - Improve the initial surface figure quality
- MEMS DM interconnect development
 - Interconnect for flight
 - Joint development between JPL flight connector engineering and BMC

- **MPIA: prototype performance**
 - Demonstrated sub-um position accuracy and 1-2 arcsecond pointing accuracy/repeatability
 - MPIA delivered a CAD model of their current design concept based on PZT actuators and DC motor & lead screw actuator
- **JPL: accommodate with redesigned optical bench**
 - Re-configured Optical prescription to better accommodate X/Y stages
 - Compact optics mounting scheme
 - Open slot in optical bench structure

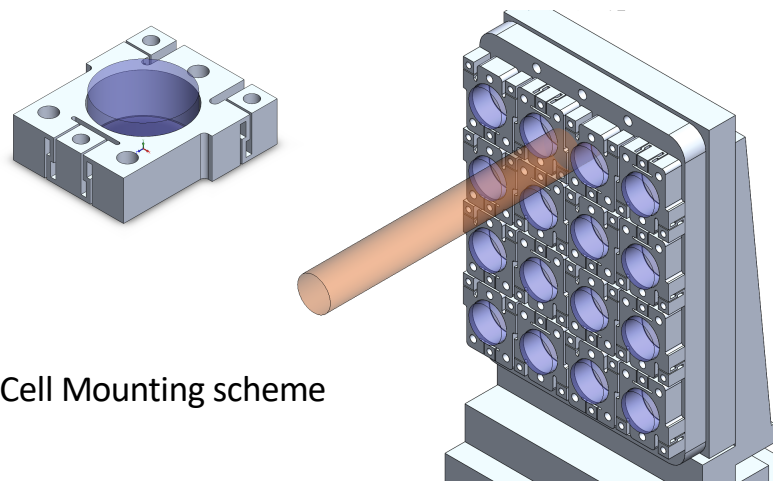
MPIA Mechanism Prototype



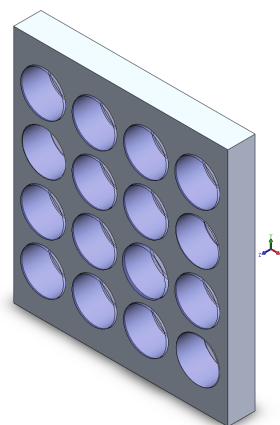
**Picture of prototype
XY-stage mechanism**

X/Y PAM Accommodation Summary w/ Direct Mounting

Mechanism	Total Number of Slots	Total Number of Spare slots	Packing [rows x columns]	Est. Volume Req w/ Cell mounting [mm x mm x mm]	Est. Volume Req w/ Direct Mounting [mm x mm x mm]	Required Cutout in bench w/ Cells? Depth?
SPAM	6	2	3x2 or 2x3	105 x 175 x ~100	105 x 175 x ~100	Y, 45 mm
FPAM	5	1 (+1)	3x2 or 2x3	165 x 175 x ~100	165 x 165 x ~100	Y, 40 mm
LSAM	6	2	3x2 or 2x3	165 x 170 x ~100	165 x 165 x ~100	Y, 40 mm
FSAM	13	3 (+1)	4x4	120 x 135 x ~100	110 x 110 x ~100	Y, 20 mm
CFAM	16	4	4x4	120 x 135 x ~100	110 x 110 x ~100	Y, 20 mm
CSAM	12	1	3x4 or 4x3	120 x 125 x ~100 Or 80 x 135 x ~100	110 x 90 x ~100 Or 80 x 115 x ~100	N if horizontal, Y, 20 mm if vertical



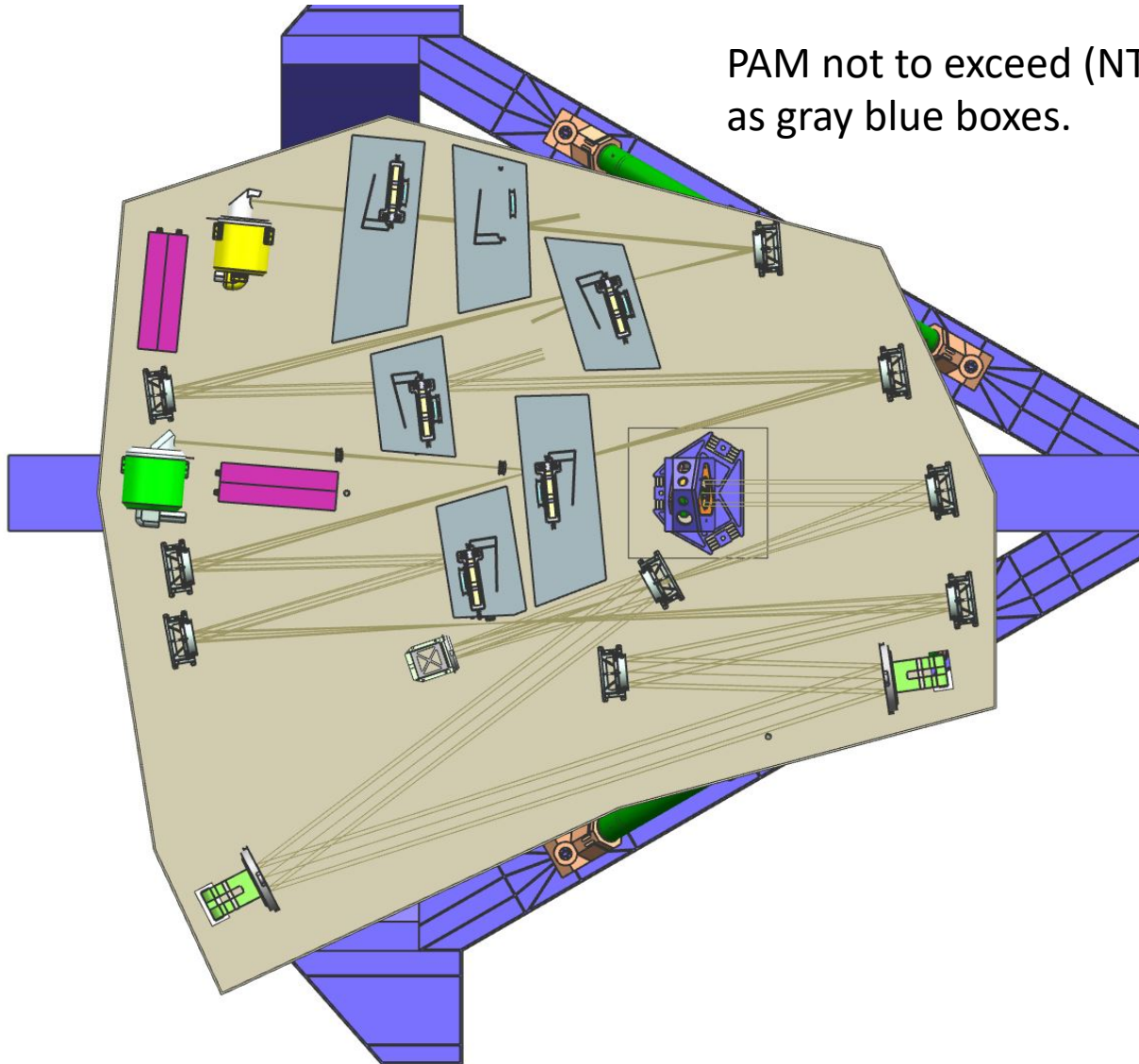
Cell Mounting scheme



Directly Bonded Optics

- Volume depends on packing efficiency of optic carriages.
- If we can bond directly to carriage, we can fit in a smaller volume
- X/Y stage feasible with new volumes but may require direct mounting to an optical tray or cutouts in bench.
- Using JPL provided optical tray with mounted optics as interface, we have better control of volume.

CGI Bench Layout and PAM NTE Volume



PAM not to exceed (NTE) volumes shown as gray blue boxes.

Opto-Mechanical Layout with Old Bench With IFS On The Other Side

